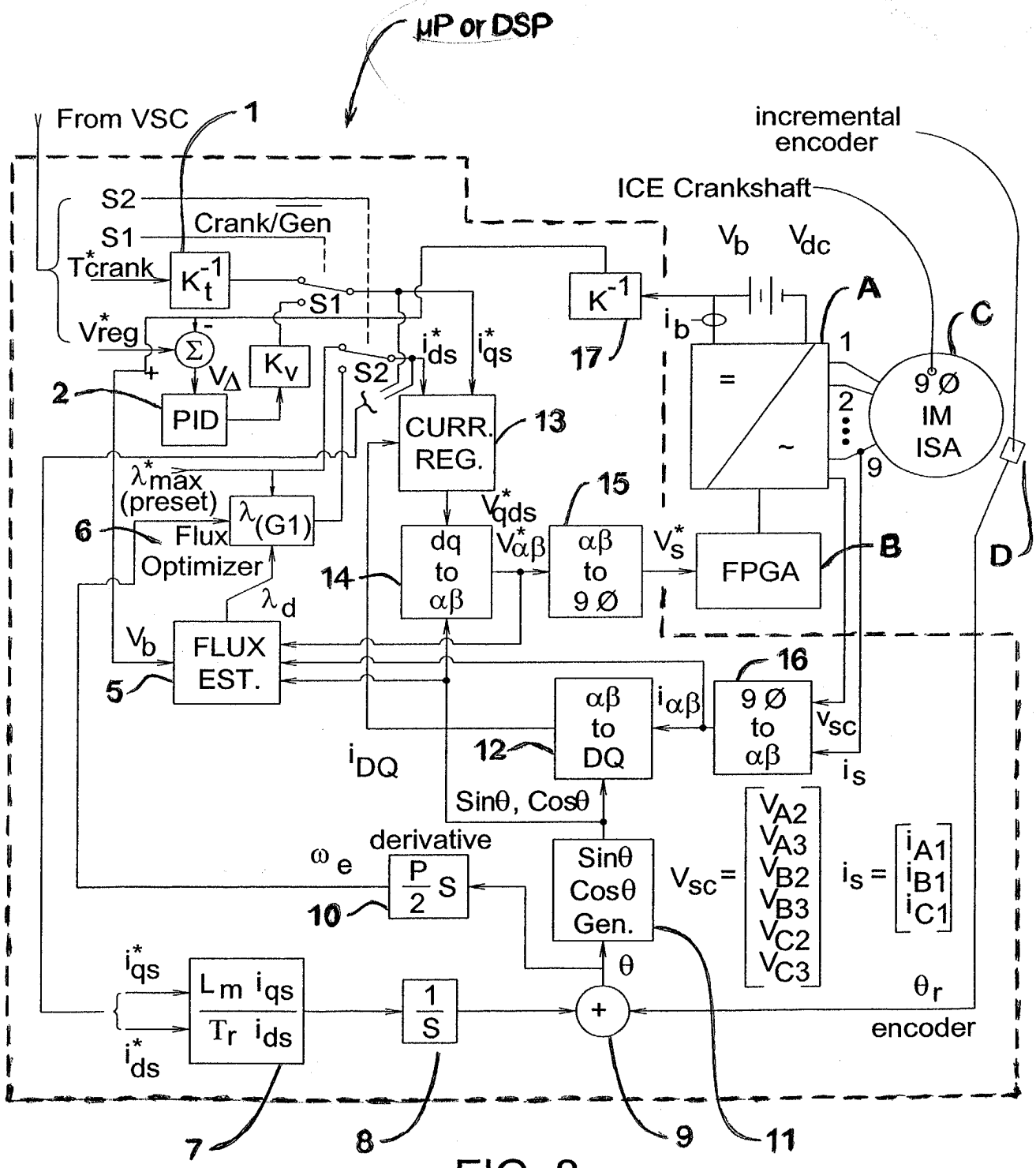
μP or DSP
From VSC
1
incremental encoder
ICE Crankshaft
S2
S1
Crank/Gen
T*crank
K_t^-1
S1
V*reg
Σ
V_Δ
K_V
S2
i*ds
i*qs
K^-1
17
V_b
V_dc
A
i_b
C
1
2
9
9 Ø IM ISA
=
~
2
PID
CURR. REG.
13
λ*max (preset)
λ(G1)
6
Flux Optimizer
λ_d
V*qds
15
dq to αβ
14
V*αβ
αβ to 9 Ø
V*s
FPGA
B
D
V_b
FLUX EST.
5
16
αβ to DQ
i_αβ
9 Ø to αβ
V_sc
i_s
12
i_DQ
Sinθ, Cosθ
derivative
ω_e
P/2 S
10
Sinθ Cosθ Gen.
V_sc = V_A2 V_A3 V_B2 V_B3 V_C2 V_C3
i_s = i_A1 i_B1 i_C1
i*qs
i*ds
Lm i_qs / Tr i_ds
7
1/S
8
θ
+
9
11
θ_r
encoder

FIG. 8